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(12) # EUROPEAN PATENT APPLICATION

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(54) **Method for manufacturimg a SOI wafer**

(57) This invention relates to a method of fabricating a SOI (Silicon-On-Insulator) wafer suitable to manufacture electronic semiconductor devices and including a substrate of monocrystalline silicon with a top surface, and a doped buried region in the substrate. The method comprises at least one step of forming trench-like openings extended from the substrate surface down to the buried region, and comprises:

- a selective etching step carried out through said openings to change said buried region of monocrystalline silicon into porous silicon;
- a subsequent step of oxidising the buried region that has been changed into porous silicon, to obtain an insulating portion of said SOI wafer.

Structure planarization by polysilicon trench filling and etchback

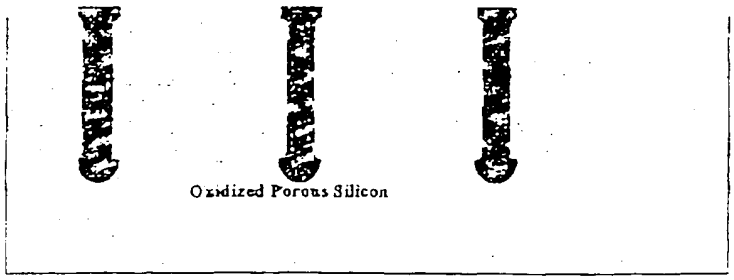


Fig. 1

EP 1 113 492 A1

Description

Field of the Invention

[0001] This invention relates to a method of fabricating a SOI (Silicon-On-Insulator) wafer suitable to manufacture semiconductor electronic devices and comprising a substrate of monocrystalline silicon having a top surface, and a doped region buried in said substrate.

Prior Art

[0002] As it is known, as an alternative to wafers made of only silicon, in recent years in the microelectronic industry have been proposed composite wafers, known as SOI wafers, which comprise at least two silicon layers, one of which being thinner than the other, and an isolation layer of silicon oxide therebetween. Reference can be made, for instance, to the article "Silicon-on-Insulator Wafer Bonding-Wafer Thinning Technological Evaluations" by J. Hausman, G. A. Spierings, U. K. P. Bierman and J. A. Pals, Japanese Journal of Applied Physics, Vol. 28, No. 8, August 1989, pages 1426-1443.

[0003] The Silicon-On-Insulator isolation technology has recently aroused considerable interest because integrated circuits having a substrate formed of SOI wafers have several advantages over circuits realised on traditional substrates made of monocrystalline silicon only. These are the main advantages:

- parasitic capacitance reduction;
- switching speed increase;
- greater immunity to noise;
- less leakage currents;
- no latch-up of parasitic components;
- greater resistance to radiation effects;
- increase of the component packaging density.

[0004] However, the application of integrated devices based on SOI substrates is severely limited in particular by the high cost of SOI wafers.

[0005] As described in the above article, a typical method of manufacturing SOI wafers comprises bonding two wafers of monocrystalline silicon together. According to such process, one of the two wafers is subjected, to an oxidation step, which allows to form an oxide layer on one surface.
The oxide layer surface is then cleaned and bonded to the other wafer.
The SOI wafers thus obtained exhibit excellent electrical characteristics but are cost-intensive.

[0006] Another method, commonly known as SIMOX (Separation by IMplants of OXygen) method, comprises the implantation of oxygen atoms into the wafer to bring the oxide thickness into the 100 to 200 nm range.

[0007] This and other methods are described in an article "SOI Technologies:
Their Past, Present and Future" by J. Haisha, Journal de Physique, Colloque C4, Supplement an N. 9, Tome 49, September 1988. Although these techniques produce the SOI structure using a single wafer, they have certain disadvantages, such as the inability to accept the application of high voltages, as in case of SIMOX technology, and the high faultiness rate due to crystallographic defects produced by the stress induced by the buried oxide.
It is also known a method of fabricating SOI wafers at a low cost, described in the European Patent No. 98830299.8, May 15, 1998, of the same Applicant. This method comprises the following steps:

- subjecting a substrate of monocrystalline silicon to a thermal oxidation step in order to grow a silicon oxide layer over its surface;
- removing certain oxide areas, whereinto ions with dopant opposite to the one of the substrate are implanted and diffused, in order to provide plural areas with dopant opposite to the one of the substrate, beneath the top surface of the substrate;
- growing an epitaxial layer with the same dopant and concentration of the substrate;
- subjecting again the semiconductor to a thermal oxidation step, and etching to define trench-like openings extending from the surface to the buried regions;
- dipping the wafer into an electrolytic solution in a galvanic cell, in which it is subjected to a selective electrochemical etching step of said areas having an opposite dopant to the one of the substrate, with porosity formation;
- subjecting the wafer to thermal oxidation, so that the porous regions are changed into oxidised regions;
- removing said oxidised regions to leave a buried cavity;
- proceeding with a new oxidation to fill the trench-like openings and said buried cavity with oxide.

[0008] Although in many ways advantageous, this method has a drawback in that the processing sequence above described is burdened with a large number of steps.

[0009] Furthermore, a fairly high rate of crystallographic defects is to be expected from such a sequence.

Since the rate of thermal oxidation is not constant along all the walls of the structure and especially at the corners thereof, some of the trench-like openings will tend to close in advance, causing a wedging effect and consequent high stress, which will be relieved through the formation of crystallographic defects.

[0010] The underlying technical problem of this invention is to provide with a low-cost method of fabricating SOI wafers showing a high yield, suitable to manufacture electronic devices monolithically integrated on a semiconductor.

Summary of the Invention

[0011] The concept behind this invention is that one of turning the doped buried region, trapped within the substrate of monocrystalline silicon, into a region of porous oxide having electrical and physical properties similar to those of a thermal oxide.

[0012] Briefly stated, according to the invention the method comprises a step of forming trench-like openings extended from the substrate surface to the buried region; a selective etching step, to be carried out through said openings in order to turn said buried region by monocrystalline silicon into porous silicon; a step of oxidising of said porous silicon to produce an insulating portion of said SOI wafer.

[0013] Based on the above concept, the technical problem is solved by a method as previously indicated and defined by the characterising part of the here attached Claim 1.

[0014] The features and advantages of the method according to this invention can be appreciated from the following description of an embodiment thereof, given by way of illustration and not of limitation with reference to the accompanying drawings.

Brief Description of the Drawings

[0015] Figures 1a-f schematically show an enlarged vertical cross-section viewof a portion of a semiconductor substrate, chronologically subjected to the various steps of the inventive method.

[0016] Figure 2a shows a SEM image of the sample in vertical cross-section, from which the effect of an electrochemical etch to produce a porous silicon region can be appreciated.

[0017] Figure 2b shows a photograph representation of an isolation layer between trenches which is approximately 20μm wide.

[0018] Figure 3 shows a TEM (Transmission Electron Microscopy) image of a porous silicon region as obtained by the method of this invention.

[0019] Figure 4 shows a TEM image of the sample, in vertical cross-section, following to an oxidation step.

Detailed Description

[0020] The process steps and the structures described hereinafter do not form an exhaustive process flow for manufacturing integrated circuits. This invention actually can be practised in combination with integrated circuit manufacturing techniques currently employed in the industry, and only such conventional commonly used process steps, necessary to understand the invention will be hereafter described.

[0021] Figures showing cross-sections through portions of an integrated circuit during its manufacture are not drawn to scale, but they rather highlight major features of the invention.

[0022] Referring to such figures, and especially to the example of Figure 1a, a substrate 2 of monocrystalline silicon, e.g. of the n type, is schematically shown at 1 which has a top surface 3 and includes a doped region 4, e.g. of the p type, buried in the substrate 2. The regions 8 represent doped regions adjacent to the buried region 4.

[0023] At location of selected areas, the substrate 2 is subjected to an etching step, for instance by an APCVD (Atmosphere Pression Chemical Vapor Deposition) process phase, which allows to define trench-like openings. In essence, an oxide 5 is first grown over the surface 3 of said substrate. Thereafter, the oxide 5 is etched away, using a mask, to form openings or trenches 6 which extend from the surface 7 of the oxide 5 down to the doped regions 8 adjacent to the buried region 4, as illustrated in Figure 1b.

[0024] Following to the formation of the trenches 6, the oxide layer 5 is removed, and the structure visible in Figure 1b is subjected to electrochemical etching as shown in Figure 1c. This type of etch is applied in an electrochemical cell 9 containing a solution of water (H_2O) and hydrofluoric acid (HF). A solvent, such as isopropyl acid, can be added to this solution.

[0025] The semiconductor structure shown in Figure 1b is placed on the anode of the cell 9, at a positive potential as to the cell cathode. By utilising the difference of potential between the substrate 2 of monocrystalline silicon and the buried region 4, and suitably modulating the dopant distribution -- for example, the dopant concentration must be at least 10^{16} atoms/cm^3 -- the doped buried region 4 is turned into a region 10 of porous silicon, obtaining a structure as shown in Figure 1d.

[0026] In addition, the electrochemical etching process has infinite selectivity, such as from 1 to 1000. In other words, the etch is only selective in the respect of the buried region 4. This is due to the fact that the electrochemical etch reactions cannot take place on the n-type region which, being at a lower potential than the p-type regions, acts as the cathode.

[0027] The porous silicon region extends all across the buried region. Accordingly, regions extending from one trench to an adjacent trench can be interconnected so that the buried doped region is formed without a con-

tinuing solution. The SEM image shown in Figure 2 illustrates the formation of the porous silicon.

[0028] Subsequently, as shown in Figure 1e, the porous silicon region formed by electrochemical etching is converted to an oxide region 11. This conversion is obtained by thermal oxidation, for example. Alternatively, an anodic oxidation within an electrolytic cell containing no HF could be applied. This oxidation step produces the oxidation of the porous silicon region, and causes a silicon oxide 12 grown also along the trench walls, as well as an oxide 13 grown at the interface between the region 11 of oxidised porous silicon and the region 2 of monocrystalline silicon. In this way, the structure shown in Figure 1e is obtained. The TEM vertical cross-section reproduced in Figure 4 shows that the whole buried region 4 has been oxidised, and that the SOI structure produced exhibits neither large defective regions nor regions of high stress.

[0029] Lastly, in a conventional way, a planarizing step is carried out on the SOI wafer to fill the trenches 6 with polysilicon, (6), and an additional etching step is applied to the polysilicon itself, yielding the SOI wafer shown in Figure 1f.

[0030] Using the method described hereinabove, SOI wafers can be produced by comparable techniques to those of the standard process employed in the microelectronics industry and, therefore, at a much lower cost than by current SOI substrate manufacturing processes and with high levels of repeatability and reliability.

[0031] Standard electronic components can be fabricated inside and/or outside the monocrystalline silicon region overlying the region of oxidised porous silicon, in accordance with standard microelectronics techniques, or different (pressure, gas, temperature, etc.) sensors, microintegrated mechanical structures such as gyroscopes, micromotors, etc..

Claims

1. A method of fabricating a SOI (Silicon-On-Insulator) wafer, suitable to manufacture electronic semiconductor devices and including a substrate of monocrystalline silicon with a top surface, and a doped region. buried in said substrate; said method comprising at least one step of forming trench-like openings extended from the substrate surface down to the buried region, and being characterised in that it further comprises:

   - a selective etching step carried out through said openings to change said buried region of monocrystalline silicon into porous silicon;

   - a subsequent step of oxidising the buried region that has been changed into porous silicon, to obtain an insulating portion of said SOI wafer.

2. A method according to Claim 1, characterised in that said selective etching step is carried out by subjecting said substrate of monocrystalline silicon to an electrochemical etching within an electrolytic cell.

3. A method according to Claim 2, characterised in that said cell contains an aqueous solution of hydrofluoric acid (HF) and a solvent to promote the formation of said porous silicon.

4. A method according to Claims 2-3, characterised in that said wafer is placed on the anode of said cell, at a positive potential as to the cathode of said cell.

5. A method according to Claim 4, characterised in that said porous silicon is obtained by utilising the difference of potential between said substrate of monocrystalline silicon and said buried region, and by modulating the dopant distribution.

6. A method according to Claim 1, characterised in that the formation of porous silicon is initiated by only one of the trenches and propagates towards the other trenches.

7. A method according to Claim 1, characterised in that the etching process resulting in the formation of porous silicon is selective only in the respect of the buried region.

8. A method according to Claim 7, characterised in that said etching process creates a smooth surface at the interface between the porous silicon region and the monocrystalline silicon one.

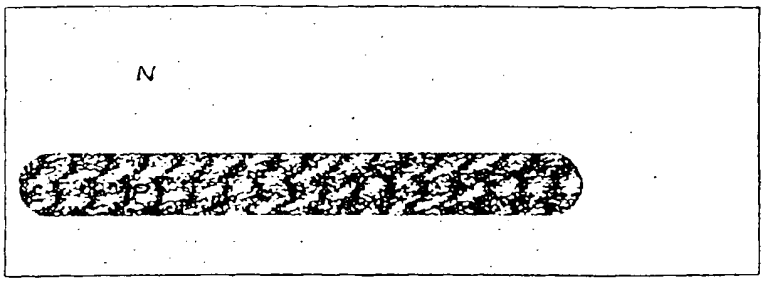
9. A method according to Claim 1, characterised in that said oxidising step is a thermal oxidation step.

10. A method according to Claim 1, characterised in that said oxidising step produces the oxidation of the porous silicon and causes the grown of the silicon oxide along the trench walls as well as along the interface between the porous silicon and monocrystalline silicon.

11. A method according to Claim 1, characterised in that it comprises a subsequent step of planarizing the SOI wafer by filling the trenches with polysilicon.

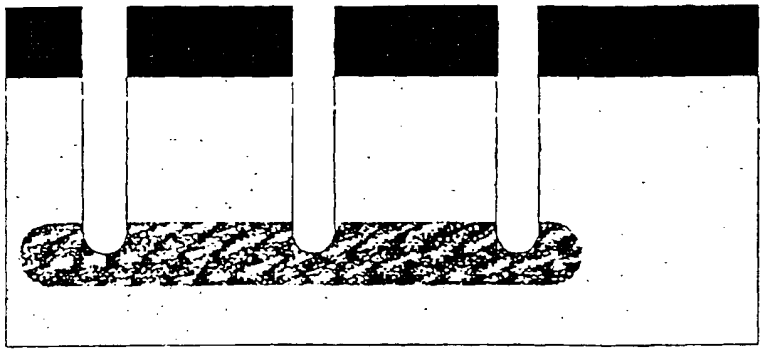
12. A method according to Claim 12, characterised in that it comprises an additional polysilicon etching step.

a)



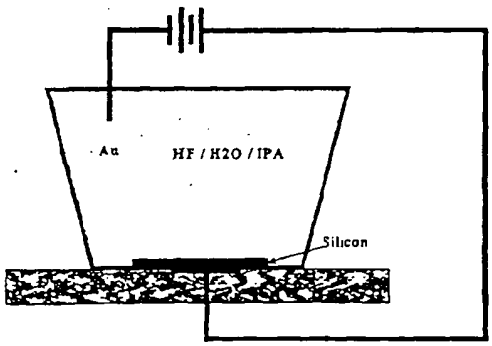
Trench etch through APCVD oxide hard mask

b)



Porous Silicon Formation

c)



Reactions:

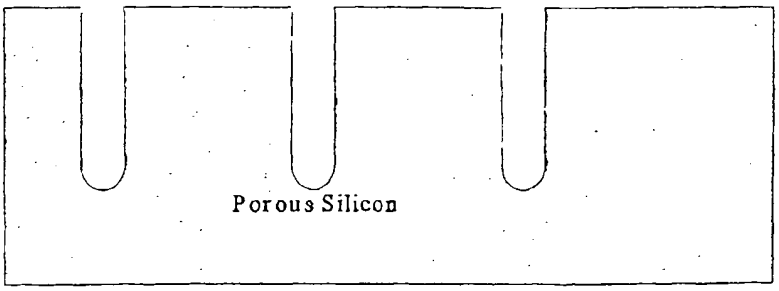
(+) $Si + 2HO + 4h \rightarrow SiO_2 + 4H$

$SiO_2 + 6HF = SiF_6^{2-} + 2HO + 2H$

(-) $H^+ + e = \frac{1}{2} H_2$

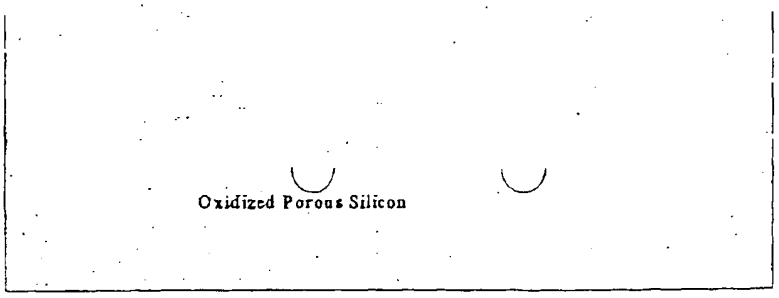
Fig. 1

d)



Thermal Oxidation

e)



Structure planarization by polysilicon trench filling and etchback

f)

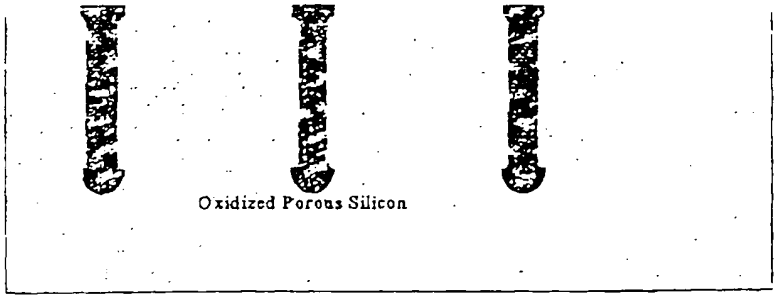


Fig. 1

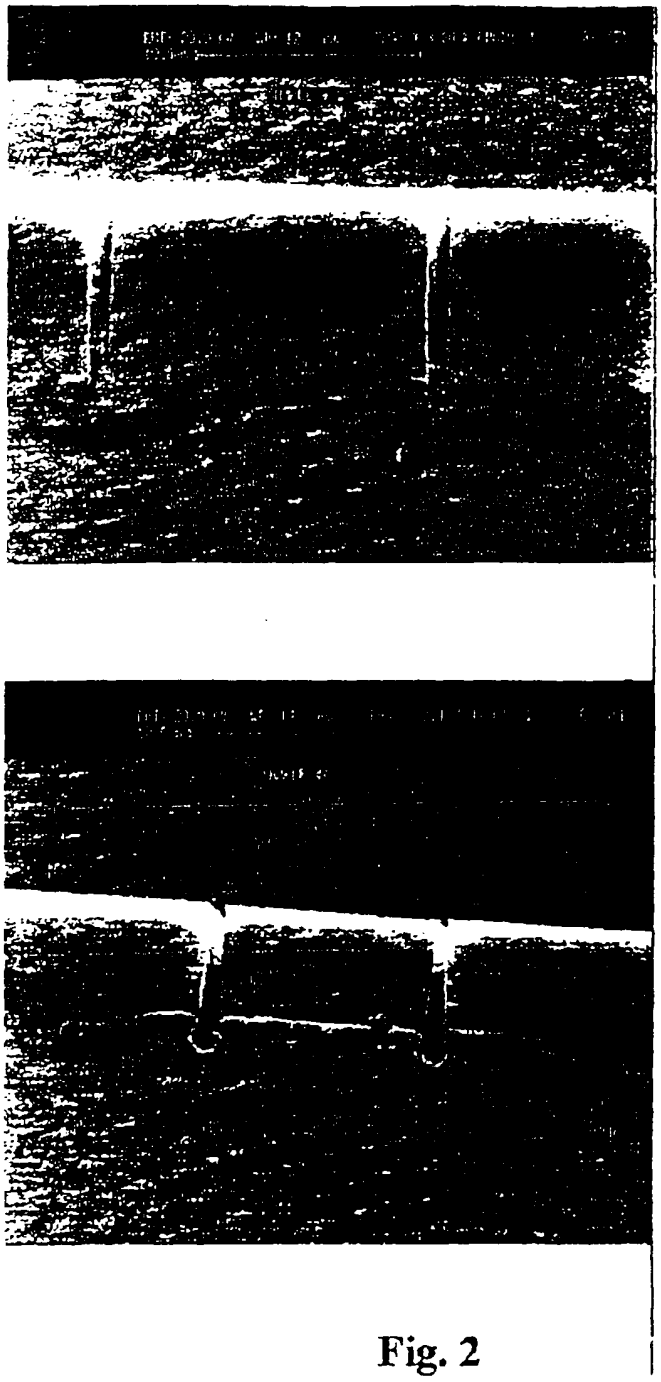


Fig. 2

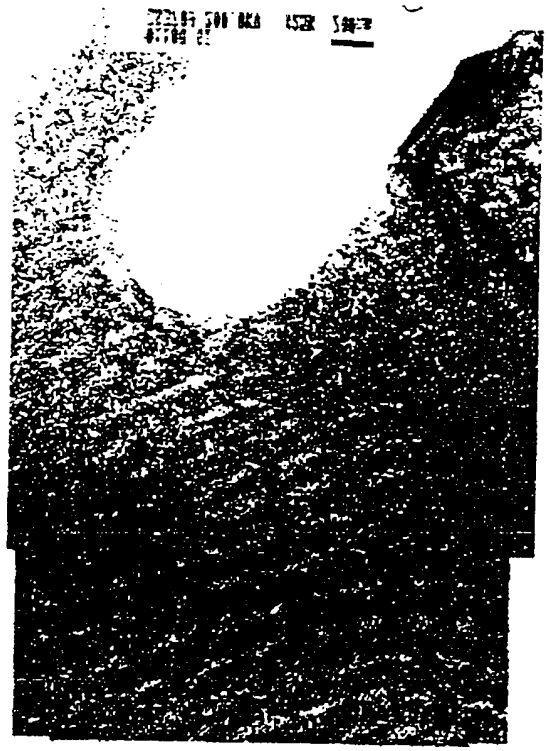


Fig. 3

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EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0826

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	FR 2 564 241 A (BOIS DANIEL) 15 November 1985 (1985-11-15) * the whole document *	1-12	H01L21/762 H01L21/316
X	EP 0 226 091 A (TEXAS INSTRUMENTS INC) 24 June 1987 (1987-06-24) * the whole document *	1-12	
X	US 5 686 342 A (LEE SEOKSOO) 11 November 1997 (1997-11-11) * abstract *	1-10	
A	WO 93 10559 A (ANALOG DEVICES INC) 27 May 1993 (1993-05-27) * abstract; figure 1 *	8-12	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	22 May 2000	Werner, A

CATEGORY OF CITED DOCUMENTS

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22-05-2000

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